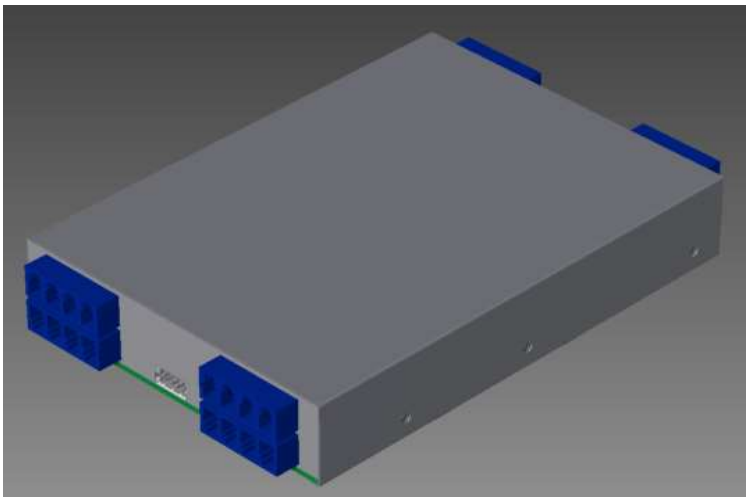

QUAD OPTICAL LINE PROTECTION TAP MODULE

OVERVIEW

The sercalo quad optical line protection tap module is a fiber optic switch based on MEMS technology. The switching mechanism offers the reliability of a solid state device.

The miniature package withstands rugged environments, dimensions and mounting holes meet EIA/ECA-740 standard (SFF-8301). The optical module communicates over I2C/SMBus interface.

The component is designed to comply Telcordia 1221 quality standards.

FEATURES

- Low insertion loss
- Low response time
- I2C/SMBus interface
- Miniature size compatible with 3.5-inch HDD

APPLICATIONS

- optical cross-connect
- optical network protection/restoration

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sercalo's quad optical line protection tap module is composed by four independent optical networks based on a series of switches and splitters (50/50 or 10/90 tap ratios). It comes with latching (option A) or non-latching (option B) fiber optic switches. The configuration of the network is controlled by an I2C/SMBus interface.

TECHNICAL SPECIFICATIONS for *Single Mode fiber*

	Unit	*Min*	*Typ*	*Max*
Optical Specifications				
Wavelength range	nm	1240	-	1640
Insertion loss (switch)[1]	dB	-	0.4	1.0
Insertion loss (50/50 splitter)[1]	dB	-	3.07	3.4
Insertion loss (switch + 50/50 splitter)[1]	dB	-	3.5	4.4
Crosstalk	dB	60	75	-
Return Loss	dB	50	55	-
Absolute optical power (switch inputs)	mW	-	-	100
Absolute optical power (splitter inputs)	mW	-	-	200
Switching time	ms	-	2	10
Durability	cycles	No wear out		
Electrical Specifications				
Supply voltage (V_{CC})	V	4.75	5	24
Power consumption	mW	-	45	1500
SMBus/I^2C bus speed	kbps	-	-	400
I2C and ADDRn low-level voltage	V	-0.5	-	0.8
I2C and ADDRn high-level voltage	V	2.5	-	5.5
$\overline{\text{RESET}}$ low-level voltage	V	-0.5	-	0.8
$\overline{\text{RESET}}$ high-level voltage	V	2.4	-	5.5
$\overline{\text{RESET}}$ minimum input pulse	µs	1	-	-
$\overline{\text{RESET}}$ glitch rejection	ns	-	100	-
Package				
Operation temperature	°C	-10	-	70
Storage temperature	°C	-40	-	85
Weight	g	TBD		
Dimensions (body)	mm	140 x 101.6 x 25.5		

[1] *Values at 25°C at 1310 or 1550 nm, without connectors.*

ORDERING INFORMATION

QUAD DUPLEX 1x2	-	50/50	-	A	-	9	LC/PC

Switch configuration

Tap ratio:
50/50
10/90

Network
A = latching
B = non-latching

Fiber type:
9 = SMF28ULTRA
(other fiber types and wavelengths upon request)

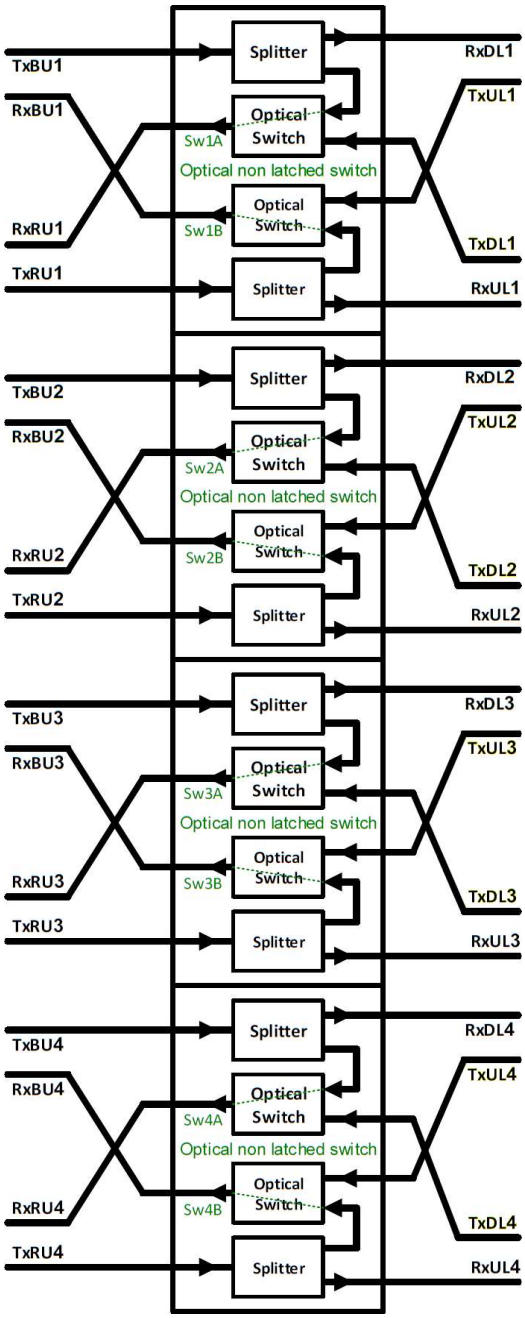
Connector type:
LC/PC

ELECTRICAL CONNECTOR PINOUT

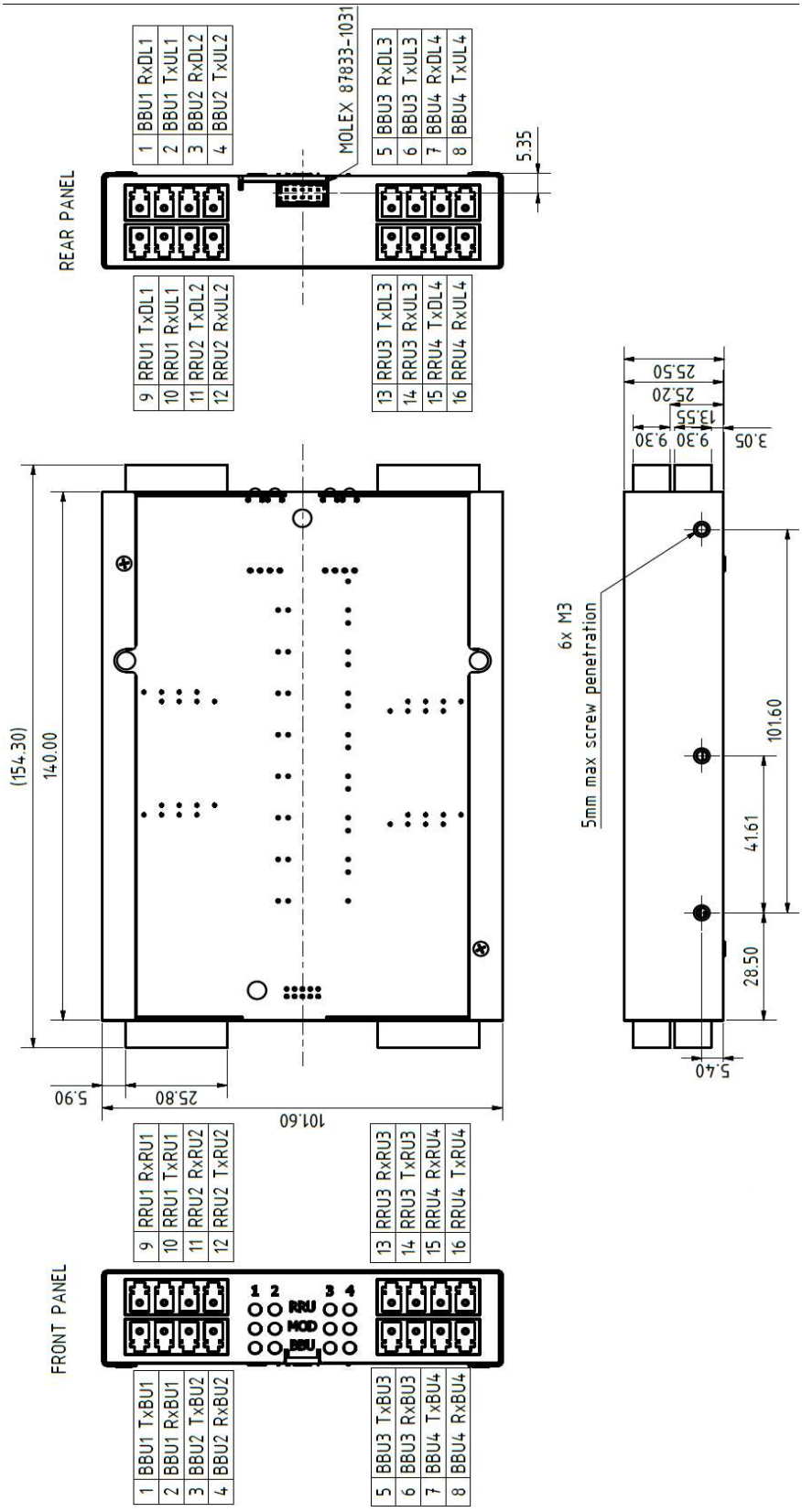
Pin number	*Description*	*Pin number*	*Description*
1	SMBus/I2C SDA	6	Reserved[3]
2	SMBus/I2C SCL	7	Reserved[3]
3	SMBus/I2C Addr0[2]	8	Reset[2]
4	SMBus/I2C Addr1[2]	9	Ground (GND)
5	SMBus/I2C Addr2[2]	10	Supply voltage (V_{CC})

[2]Signal connected to +3.3V through internal 10kohm pull-up resistor
[3]Let reserved pins unconnected.

FUNCTIONAL BLOC DIAGRAM (50/50 SPLITTER OPTION)



PRODUCT DIMENSIONS (IN MILLIMETERS)



I2C/SMBUS ADDRESS MAP

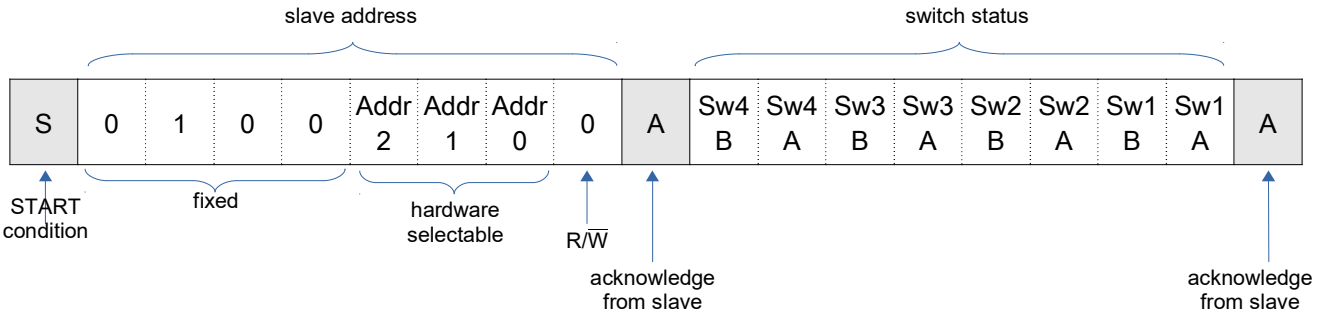
Addr2	*Addr1*	*Addr0*	*Address of optical switches control (hex)*	*Address of signaling LEDs control (hex)*
0	0	0	20h	C0h
0	0	1	21h	C1h
0	1	0	22h	C2h
0	1	1	23h	C3h
1	0	0	24h	C4h
1	0	1	25h	C5h
1	1	0	26h	C6h
1	1	1	27h	C7h

ADDRESS OF SIGNALING LEDS

Address	*LED*
0	RRU1 Green
1	MOD1 Green
2	MOD1 Yellow
3	BBU1 Green
4	RRU2 Green
5	MOD2 Green
6	MOD2 Yellow
7	BBU2 Green
8	RRU3 Green
9	MOD3 Green
10	MOD3 Yellow
11	BBU3 Green
12	RRU4 Green
13	MOD4 Green
14	MOD4 Yellow
15	BBU4 Green

- Refer to NXP PCA9552 for additional details on timing and transmission protocol

CONFIGURING OPTICAL SWITCHES



- Switch status bit 0: CROSS
  Switch status bit 1: BAR (default at startup and power off, green path on functional block diagram)
- Refer to NXP PCA9670 for additional details on timing and transmission protocol